Claims

[c1] 1. A signal jitter measuring device for quantifying a jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, wherein the phase locked loop provides a first phase difference signal and a second phase difference signal therein, said measuring device comprising:
a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between said output signal and said input signal of the phase locked loop; and
a jitter-level output unit coupled to said phase-relationship detection unit and responsive to said first phase difference signal, said second phase difference signal and said phase relationship signal for generating a jitter-level output signal that corresponds to the level of jitter between said output signal and said input signal of the phase locked loop;
wherein said jitter-level output signal is a pulse width difference between said first phase difference signal and said second phase difference signal.

[c2] 2. The signal jitter measuring device of claim 1, wherein the phase-relationship detection unit comprises:
a triggering unit responsive to said input signal of the phase locked loop for generating a triggering signal; and
a D-type flip-flop taking said output signal of the phase locked loop as its input data and said triggering signal as its input clock to produce said phase relationship signal.

[c3] 3. The signal jitter measuring device of claim 2, wherein the triggering unit includes:
a delay circuit for delaying said input signal to produce a delayed input signal; and
a XOR gate for receiving said input signal and said delayed input signal and producing said triggering signal.

[c4] 4. The signal jitter measuring device of claim 1, wherein the jitter-level output unit includes:

a first multiplexer for receiving said first phase difference signal, said second phase difference signal and said phase relationship signal, and selectively outputting said second phase difference signal when said phase relationship signal indicates the phase of said output signal leads said input signal, and selectively outputting said first phase difference signal when said phase relationship signal indicates the phase of said output signal lags behind the input signal;

a second multiplexer for receiving said first phase difference signal, said second phase difference signal and said phase relationship signal, and selectively outputting said first phase difference signal when said phase relationship signal indicates the phase of said output signal leads said input signal, and selectively outputting said second phase difference signal when said phase relationship signal indicates the phase of said output signal lags behind said input signal;

a first low-pass filter for converting the output of said first multiplexer into a first low-pass output signal;

a second low-pass filter for converting the output of said second multiplexer into a second low-pass output signal; and

a subtraction unit for receiving said first low-pass output signal and said second low-pass output signal which computes said pulse width difference between said first phase difference signal and said second phase difference signal and produces said jitter-level output signal.

[c5] 5. The signal jitter measuring device of claim 4, wherein the first low-pass filter and the second low-pass filter are RC low-pass filtering circuits.

[c6] 6. The signal jitter measuring device of claim 1, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next trigger transition point of said output signal after the generation of said second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition point of said output signal after the data transition of said input signal, and the second phase difference signal is maintained for a full cycle of said output signal.

[c7] 7. The signal jitter measuring device of claim 1, wherein the first phase

difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, the second phase difference signal is asserted at the triggering transition points of said output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.

[c8] 8. A phase locked loop having an input signal and an output signal, and capable of providing information on signal jitter, said phase locked loop comprises:
a phase detection circuit in respond to said input signal and said output signal for providing a first phase difference signal and a second phase difference signal; and
a signal jitter measuring device coupled to said phase detection circuit and responsive to said first phase difference signal and said second phase difference signal for generating a jitter-level output signal that corresponds to the jitter level between said input signal and said output signal of said phase locked loop;
wherein said jitter-level output signal is related to the difference in pulse width between said first phase difference signal and said second phase difference signal.

[c9] 9. The phase locked loop of claim 8, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next triggered transition points of said output signal after the generation of said second phase difference signal, the second phase difference signal is asserted at the next non-triggered transition points of said output signal after data transition of said input signal, and said second phase difference signal is maintained for a full cycle of said output signal.

[c10] 10. The phase locked loop of claim 8, wherein said first phase difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, and said second phase difference signal is asserted at said triggering transition points of said

output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.

[c11] 11. The phase locked loop of claim 8, wherein the signal jitter measuring device comprises:
a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between said output signal and said input signal of the phase locked loop; and
a jitter-level output unit coupled to said phase-relationship detection unit and responsive to said first phase difference signal, said second phase difference signal and said phase relationship signal for generating said jitter-level output signal.

[c12] 12. The phase locked loop of claim 11, wherein the phase-relationship detection unit comprises:
a triggering unit responsive to said input signal of said phase locked loop for generating a triggering signal; and
a D-type flip-flop taking said output signal of said phase locked loop as its input data and said triggering signal as its input clock to produce said phase relationship signal.

[c13] 13. The phase locked loop of claim 12, wherein the triggering unit includes:
a delay circuit for delaying said input signal to produce a delayed input signal; and
a XOR gate for receiving said input signal and said delayed input signal and producing said triggering signal.

[c14] 14. The phase locked loop of claim 11, wherein the jitter-level output unit includes:
a first multiplexer for receiving said first phase difference signal, said second phase difference signal and said phase relationship signal, and selectively outputting said second phase difference signal when said phase relationship signal indicates the phase of said output signal leads said input signal, and selectively outputting said first phase difference signal when said phase relationship signal indicates the phase of said output signal lags behind the

input signal;
a second multiplexer for receiving said first phase difference signal, said second phase difference signal and said phase relationship signal, and selectively outputting said first phase difference signal when said phase relationship signal indicates the phase of said output signal leads said input signal, and selectively outputting said second phase difference signal when said phase relationship signal indicates the phase of said output signal lags behind said input signal;
a first low-pass filter for converting the output of said first multiplexer into a first low-pass output signal;
a second low-pass filter for converting the output of said second multiplexer into a second low-pass output signal; and
a subtraction unit for receiving said first low-pass output signal and said second low-pass output signal, which computes the difference in pulse width between said first phase difference signal and said second phase difference signal and produces said jitter-level output signal.

[c15] 15. The phase locked loop of claim 14, wherein the first low-pass filter and the second low-pass filter are RC low-pass filtering circuits.

[c16] 16. A method of measuring signal jitter which is capable of quantifying the jitters between an input signal and an output signal of a phase locked loop, comprising the steps of:
providing a first phase difference signal and a second phase difference signal;
acquiring a phase relationship signal capable of showing whether the phase of said output signal leads or lags said input signal; and
acquiring a jitter value indicating the difference in pulse width between said first phase difference signal and said second phase difference signal according to said phase relationship signal.

[c17]

17. The method of claim 16, wherein the first phase difference signal is asserted at the data transition points of said input signal and de-asserted at the next triggering transition points of said output signal after the generation of said second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition points of said output signal after

data transition of said input signal and the second phase difference signal is maintained for a full cycle of said output signal.

[c18] 18. The method of claim 16, wherein the first phase difference signal is asserted at the triggering transition points of said input signal when the phase of said input signal leads said output signal and de-asserted at subsequent triggering transition points of said output signal, and the second phase difference signal is asserted at the triggering transition points of said output signal when said input signal lags behind said output signal and de-asserted at subsequent triggering transition points of said input signal.